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A Novel Asymmetrical Multilevel Inverter with Switched Capacitor Units for AC Motor

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ABSTRACT: Multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, dv/dt stresses, and stresses in the bearings of a motor. Moreover the advantages like high quality power output, low switching losses, low electro-magnetic interference (EMI) and high output voltage made multilevel inverter as a powerful solution in converter topology. In this paper two new topologies have been proposed for multilevel inverters. The proposed topologies consist of a combination of the conventional series and the switched capacitor inverter units. The proposed method introduces 17, 25 levels and three phase 25level Inverter, With the use of high level inverter, resolution is increase and also the harmonics is highly reduced. The simulation results are presented by using Matlab/Simulink software.

KEYWORDS: Multilevel inverter, series inverters, series– parallel connection, switched capacitor.

I.INTRODUCTION

Multilevel inverters have been under research and development for more than three decades and have found successful industrial applications. However, this is still a technology under development, and many new contributions and new commercial topologies have been reported in the last few years. Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations [1]. A multilevel converter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, dv/dt stresses, and stresses in the bearings of a motor. Several multilevel converter topologies have been also developed i) diode clamped, ii) flying capacitors, and iii) cascaded or H-bridge. Referring to the literature reviews, the cascaded multilevel inverter (CMI) with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications due to their modularization and extensibility [2].

The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform [3-10]. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency Pulse Width Modulation (PWM).Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced [11], .The proposed topologies have a modular structure and can benefit the advantages of the series multilevel inverters . The fundamental switching method is used in this investigation. In addition, to produce all voltage levels at the output (even and odd), a new algorithm for the determination of the magnitude of the isolated dc voltage sources is proposed. Finally, the loss calculation is done, and the performance of the proposed topologies is verified by simulation results of single-phase 25- and 17-level inverters.

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II.PROPOSED SWITCHED CAPACITOR TOPOLOGY

Fig.1. shows the proposed switched capacitor unit. This topology is yield from series combination of several basic units. In this figure, the switches Si (i=1, 2, n) connect the capacitors in series, and the switches P_i connect the capacitors in parallel with the dc voltage sources. To produce zero and negative voltage levels, an H-bridge has been used at the output. The blocked voltage by each switch in Fig.1. is V_{dc}.

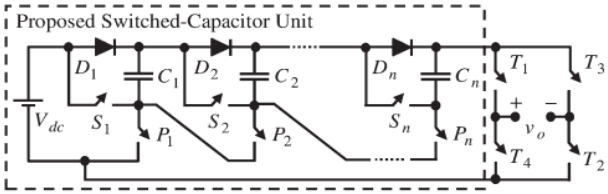

Fig.1. Proposed Switched Capacitor Unit.

Thus, the proposed switched capacitor unit is also proper for a high frequency application that is not the aim of this paper. The other advantage of the proposed topology is the boosting ability of the input dc voltage without using any transformer. This feature reduces the size and cost of the system and increases its efficiency. The maximum numbers of output voltage levels (N-step), required insulated-gate bipolar transistors (IGBTs) (NIGBT), and diodes (N-diode) for the proposed topology shown in 3.3 are calculated by the following equations, respectively,

$$N_{step} = 2n + 3 \quad (1)$$

$$N_{IGBT} = 2n + 4 \quad (2)$$

$$N_{diode} = n \quad (3)$$

Where n is the number of capacitors. The maximum output voltage that can be produced ($V_{o,max}$) is equal to

$$V_{0,max} = (n + 1)V_{dc} \quad (4)$$

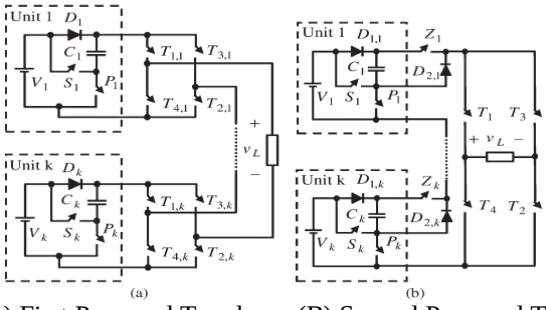

Fig.2. (A) First Proposed Topology. (B) Second Proposed Topology.

The general form of the equations that show the number of voltage levels and the number of IGBTs can be expressed as follows:

$$N_{step} = a\left[\prod_{j=1}^{k}(bn_j + c)\right] + d \quad (5)$$

$$N_{IGBT} = 2\left(\sum_{j=1}^{k} n_j\right) + ek + f \quad (6)$$

Where a, b, c, d, e, and fare the integer numbers that depend on the unit connection order. In order to produce the maximum number of voltage levels at the output with using a specified number of IGBTs, (6) can be rewritten as follows:

$$N_{IGBT} = 2(n_1 + n_2 + \cdots + n_k) + ek + f = cte \quad (7)$$

$$n_1 + n_2 + \cdots + n_k = \frac{N_{IGBT} - ek - f}{2} = cte \quad (8)$$

Considering (5) and (8), the number of voltage levels in (5) will be maximum when the following condition is satisfied

$$n_1 = n_2 = \cdots = n_k = n \quad (9)$$

From (8)–(10), Nstep is obtained as follows

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$$N_{step} = a(bn + c)^{\frac{N_{IGBT}-f}{2n+e}} + d \qquad (10)$$

Equation (10) will be maximum when nets its minimum value. Thus, the proposed topologies produce the maximum number of voltage levels at the output form=1. This result is independent of the units' connection order. The proposed topologies have been presented in the next sections with considering n=1.

A. First Proposed Topology

Fig.2.(a) shows the first proposed topology. In this topology, the switched capacitor units have been connected in series by using H-bridges. Each unit can only produce positive voltage levels. The H-bridge produces zero and negative voltage levels. There are a lot of ways to determine the magnitude of the dc voltage sources. Some of these algorithms are not able to produce all voltage levels at the output, and some of them produce repetitive voltage levels. In order to prevent the mentioned problems and produce the maximum number of voltage levels, the magnitude of the dc voltage sources in the j_{th} unit can be as follows:

$$V_j = (5^{j-1})V_1 \qquad (11)$$

Voltage and current ratings of the switches in a multilevel inverter play important roles in the total cost of the inverter. In all topologies, the currents of all switches are equal to the rated current of the load. This is, however, not the case for the voltage. Hence, there is a need for a criterion to evaluate the multilevel inverter from the viewpoint of blocked voltage by power switches and the total cost of system. This criterion is captioned as "standing voltage". The standing voltage is equal to the sum of all blocked voltages by power switches in a converter. The standing voltage of the switches is equal to the sum of the blocked voltages by switches S and P and the H-bridge switches for all units.

B. Second Proposed Topology

Fig.2. (b) shows the second proposed topology. In this topology, each unit is bypassed when the switch P_j and the diode $D_{2,j}$ are on and the switch Z_j is off. When the switch Z_j is on, the diode $D_{2,j}$ becomes reverse biased. Thus, the diode $D_{2,j}$ prevents the backward current flowing during the unit bypassing when an inductive load is used at the output. In other words, the second proposed topology can produce the desirable voltage waveforms for resistive loads. On the other hand, by replacing the diode $D_{2,j}$ with a power electronic switch, the second proposed topology can be used for resistive-inductive loads. The magnitude of the dc voltage sources and the number of voltage levels can be calculated as follows:

$$V_j = (3^{j-1})V_1 \qquad (12)$$

The number of voltage levels (N_{step}), the number of required IGBTs (NIGBT), the number of diodes (N_{diode}), the maximum output voltage (Vo, max), the standing voltage of the switches (V_{st} and), the number of dc voltage sources (N_{dc}), and the variety of the dc voltage source magnitude ($N_{variety}$) can b calculated for the first and second proposed topologies, as shown in Table I.

III. COMPARISON OF THE PROPOSED TOPOLOGIE SWITH OTHER CONVENTIONAL TOPOLOGIES

In this section, the first proposed topology has been compared with three main topologies of multilevel inverters, namely, the diode-clamped multilevel one, capacitor Clamped multilevel one, and cascaded multi cell multilevel one. Also, the proposed topology has been compared with a cascade-boost switched capacitor converter multilevel inverter, a switched capacitor boost multilevel inverter, and a hybrid-source switched capacitor multilevel inverter [9]. Table II shows the numbers of switches, diodes, capacitors, and voltage levels for the proposed topology and the topologies presented in [9]. Table II proves the advantages of the proposed topology. In order to show the advantages of the proposed topologies in comparison with some recently presented topologies that use isolated dc voltage sources.

The proposed topologies have been compared with the cascaded multilevel inverter using bidirectional switches (CMIBS), cascaded multilevel inverter using binary units (CMIBU), optimal topologies for cascaded sub multilevel inverters (OCSMI), cascaded multilevel inverter with reduced number of components for high-voltage applications (CMIHV), multilevel inverter with reduced number of power electronic components (MIRC) , and multilevel inverter using switched series/parallel dc voltage sources (MISSP) from different aspects. Fig.3. shows the number of required

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IGBTs for producing specified voltage levels at the output of the proposed topologies and the topologies presented. As can be seen, the proposed topologies need fewer IGBTs for realized Nstep voltage levels at the output.

Table I
Calculation of Different Parameters of the Proposed Topologies

Parameter	Proposed Topology	
	First	Second
N_{step}	5^k	$(2X3^k)-1$
N_{IGBT}	6^k	3k+4
N_{diode}	k	2k
$V_{0,max}$	$2\sum_{j=1}^{k} V_j$	$2\sum_{j=1}^{k} V_j$
V_{stand}	$10(1+5+\ldots+5^{k-1})V_1$ $=5\left[\frac{5^k-1}{2}\right]V_1$	$11(1+3+\ldots+3^{k-1})V_1$ $=11\left[\frac{3^k-1}{2}\right]V_1$
N_{dc}	k	k
$N_{variety}$	k	k

Table I. shown as The number of voltage levels (N_{step}), the number of required IGBTs (N_{IGBT}), the number of diodes (N_{diode}), the maximum output voltage ($V_{o,max}$), the standing voltage of the switches (V_{stand}), the number of dc voltage sources (N_{dc}), and the variety of the dc voltage source magnitude ($N_{variety}$) can be calculated for the first and second proposed topologies.

Table II
Comparison of the First Proposed Topology With The Topologies Presented

Topologies	N_{step}	N_{switch}	N_{diode}	$N_{capacitor}$	N_{dc}
First topology	25	12	2	2	2
DCM	13	24	132	12	1
CCM	13	24	0	66	1
CMM	13	24	0	6	1
CBSCM	13	10	12	6	1
SCBM	13	11	3	2	1
HSSCM	13	21	4	5	3

Table II shows the numbers of switches, diodes, capacitors, and voltage levels for the proposed topology and the topologies presented and proves the advantages of the proposed topology.

IV.MATLAB/SIMULINK RESULTS

Here simulation results are presented for (i) Single phase 17-level inverter (ii)single phase 25-level inverter (iii) three phase 25-level inverter17-level inverters.

Case i: Single Phase 17-level inverter

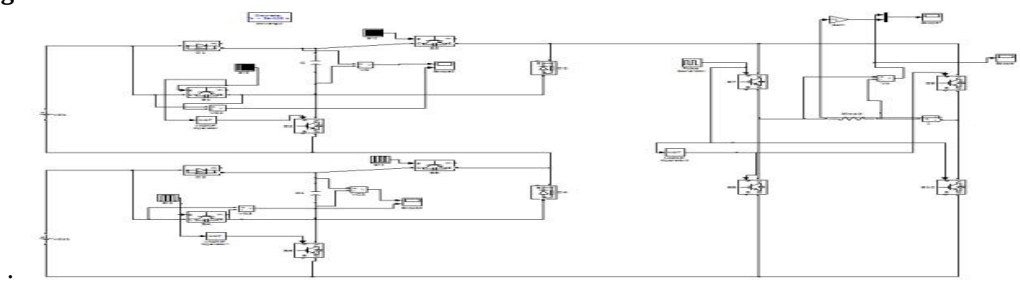

Fig.4.Matlab/Simulink model of 17-level inverter based proposed topology.

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In the fig.4 shows designing of 17-level inverter , The total harmonic distortion (THD) of the simulated 17-level load voltages. Due to low-pass filtering characteristic of the R –L, the load current is almost sinusoidal and contains less high-order harmonics than the output voltage.

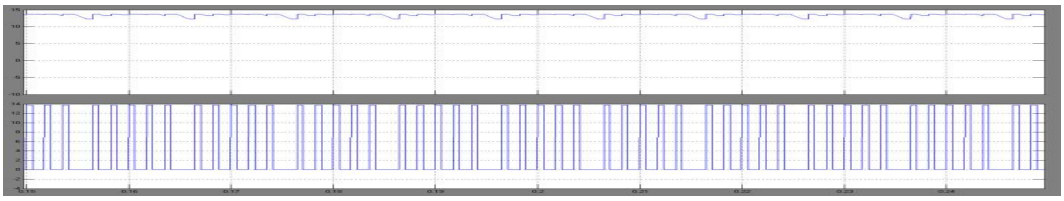

Fig.5. capacitor voltage (Vc1) and switch voltage(S1).

In the fig.5 shows capacitor voltage (Vc1) and switch voltage(S1) of measured values for 17 Level inverter. shows the capacitor voltage ripples for four cycles. The maximum voltage ripple occurs when the switch S is on.

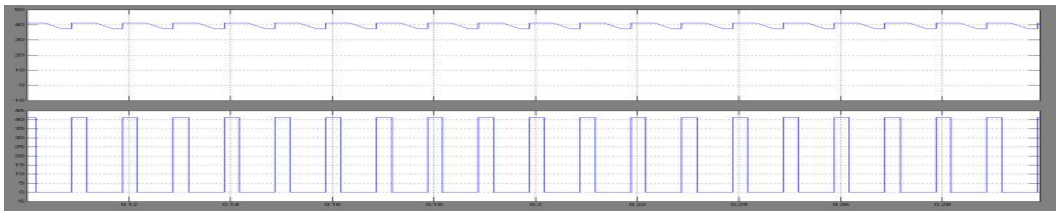

Fig. 6. capacitor voltage(Vc2) and switch voltage(S2).

In the fig.6 shows capacitor voltage(Vc2) and switch voltage(S2) of measured values for 17 Level inverter. shows the capacitor voltage ripples for four cycles. The maximum voltage ripple occurs when the switch S is on.

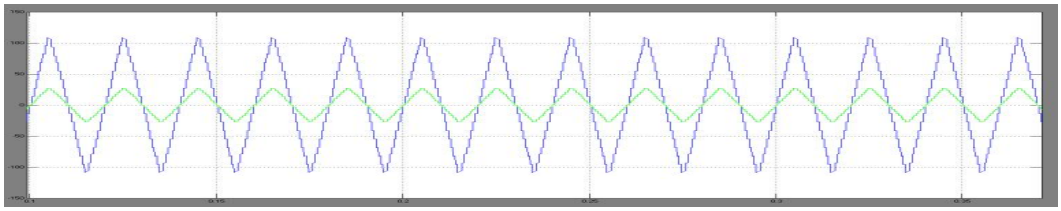

Fig.7. Simulated load voltage and current waveforms for 17-level inverter.

In the fig.7 shows Simulated load voltage and current waveforms for 17-level inverter of experimental results of the 17-level inverters for the load voltage and current, the capacitor voltage ripples. The experimental results have a good agreement with the simulation results.

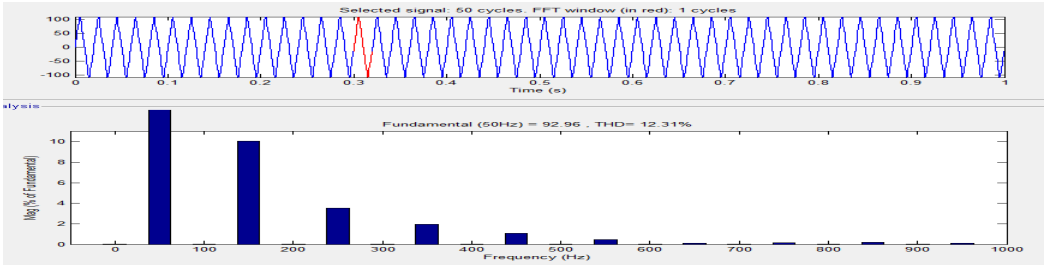

Fig.8.total harmonic distractions for 17 Level inverter.

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In the fig.8 shows Total harmonic distractions of 17 Level inverter, Due to low-pass filtering characteristic of the R –L, the load current is almost sinusoidal and contains less high-order harmonics than the output voltage.

Case ii: Matlab circuit of 25-level inverter

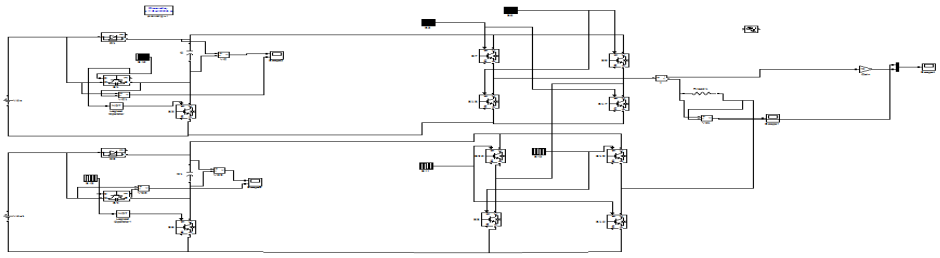

Fig.9.Matlab/Simulink model of 25-level inverter based proposed topology.

In the fig.9 shows designing of 25-level inverter , The total harmonic distortion (THD) of the simulated 25- level load voltages. Due to low-pass filtering characteristic of the R –L, the load current is almost sinusoidal and contains less high-order harmonics than the output voltage.

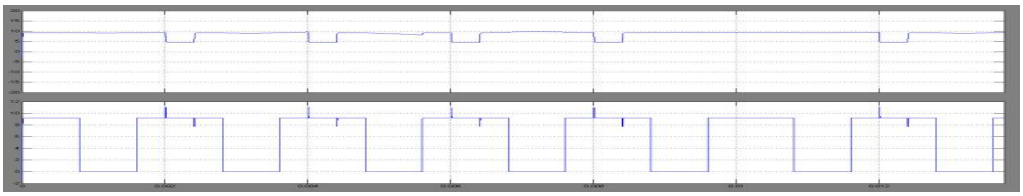

Fig. 10 capacitor voltage (Vc1) and switch voltage (S1).

In the fig.10 shows capacitor voltage (Vc1) and switch voltage(S1) of measured values for 25 Level inverter. shows the capacitor voltage ripples for four cycles. The maximum voltage ripple occurs when the switch S is on.

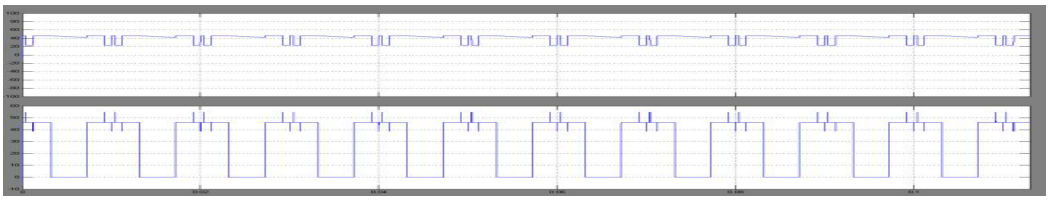

Fig.11.capacitor voltage (Vc2) and switch voltage (S2).

In the fig.11 shows capacitor voltage(Vc2) and switch voltage(S2) of measured values for 25 Level inverter. shows the capacitor voltage ripples for four cycles. The maximum voltage ripple occurs when the switch S is on.

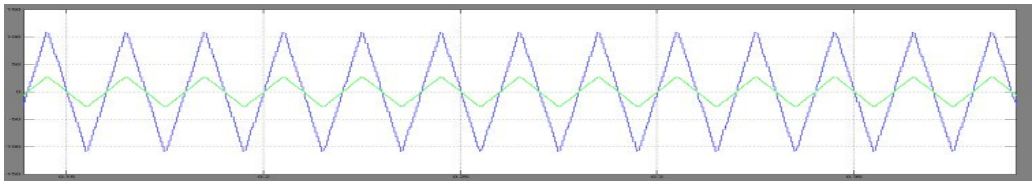

Fig.12. Simulated load voltage and current waveforms for 25-level inverter Decisive

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In the fig.12 shows Simulated load voltage and current waveforms experimental results of the 25- -level inverters for the load voltage and current the capacitor voltage ripples. The experimental results have a good agreement with the simulation results.

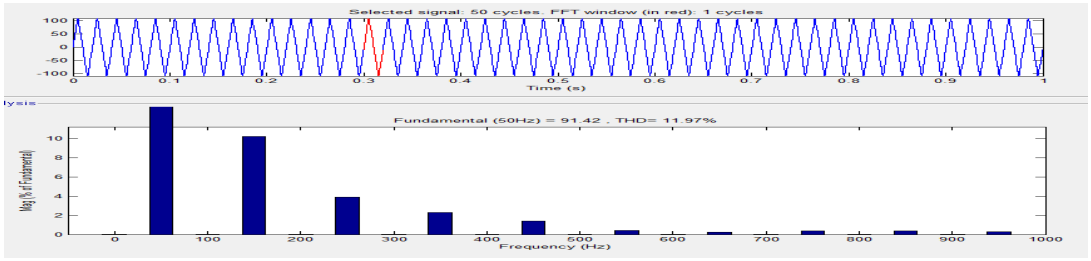

Fig.13.total harmonic distractions for 25 Level inverter.

In the fig.13 shows Total harmonic distractions of 25 Level inverter, here we are getting very low value of THD, compare to the 11-level THD value is low then we get more efficiency than 11-level. Due to low-pass filtering characteristic of the R –L, the load current is almost sinusoidal and contains less high-order harmonics than the output voltage.

Case iii: Three phase 25-level inverter with Induction Motor

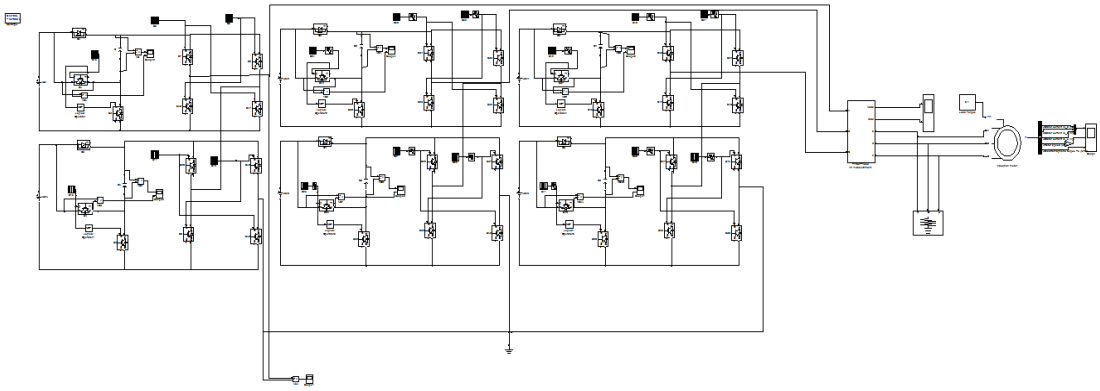

Fig.14.Matlab/Simulink Model of three phase 25-level inverter based Proposed Topology

In the fig.14 shows 25 Level inverter is to be connected three phase induction motor and finding it's performance characteristics like induction motor voltage, speed and torque.

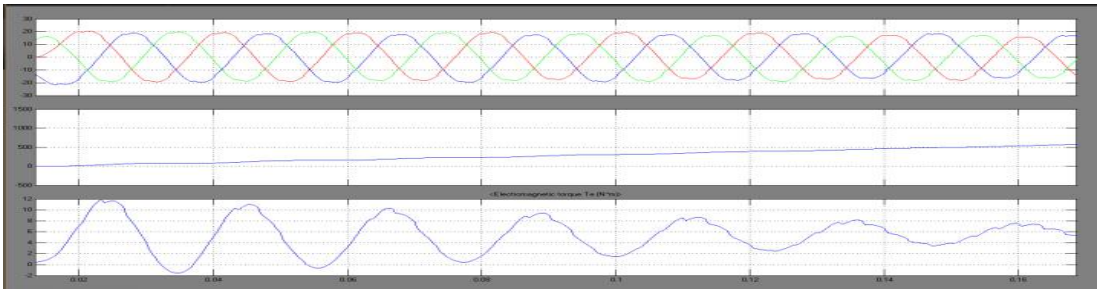

Fig 15. Three Phase voltage and three phase IM voltage, speed and torque for 25-level inverter

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In the fig.15 shows 25 Level inverter is to be connected three phase induction motor and it's performance characteristics of voltage, speed and torque are induction motor finding. Compare to the 11-level inverter best performance gives the 25-level inverter.

V. CONCLUSION

The drive system can be used in industries where adjustable speed drives are required to produce output with reduced harmonic content. The simulation results of voltage, current, speed and spectrum are presented. The number of on–off times in one cycle and the conduction intervals offal switches have been calculated as a function of the output voltage levels. The proposed topologies reduce the number of switches and isolated dc voltage sources, the variety of the dc voltage source values, and size and cost of the system in comparison with conventional series topologies. The first proposed topology produces a 25-level voltage for all load power factors by using 12 IGBTs, 2 diodes, and 2 isolated dc voltage sources. It is also observed that the proposed topology decreased the number of required power electronic switches compared to a cascaded H-bridge inverter to obtain the same 17 and 25 level output voltage with lower THD.

REFERENCES

[1] K. Bandara, T. Sweet, and J. Ekanayake, "Photovoltaic applications for off-grid electrification using novel multi-level inverter technology with energy storage," Renew. Energy, vol. 37, no. 1, pp. 82–88, Jan. 2012.
[2] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energybalance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs,"IEEE Trans. Ind. Electron., vol. 60, no. 1, pp. 98–111, Jan. 2013.
[3] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system, "IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2435–2443, Jun. 2011.
[4] A. K. Pandam and Y. Suresh, "Performance of cascaded multilevel inverter by employing single and three-phase transformers, "IET Power Electron., vol. 5, no. 9, pp. 1694–1705, Nov. 2012.
[5] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/ parallel conversion with inductive load,"IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 878–887, Feb. 2012.
[6] P. Roshankumar, P. P. Rajeevan, K. K.Mathew, J. I. Gopakumar, and L. G. Leon, "A five-level inverter topology with single dc supply by cascading a flying capacitor inverter and an H-bridge,"IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3505–3512, Aug. 2012.
[7] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulse width modulation,"IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1517–1526, Jun. 2010.
[8] Y. Ounejjar, K. A. Haddad, and L. A. Gregoire, "Packed U-cells multilevel converter topology: Theoretical study and experimental validation,"IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1294–1306, Apr. 2011.
[9] S. Ding, M. Cheng, Z. Wang, K. T. Chau1, Y. Wang, and W. Wang, "A hybrid-source switched-capacitor multilevel converter for electric vehicles," in Proc. ICEMS, Incheon, South Korea, 2010, pp. 288–292.

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